



# International Journal of Multidisciplinary Research in Science, Engineering and Technology

*(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)*



**Impact Factor: 8.206**

**Volume 9, Issue 3, March 2026**



## International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

# Static Random Access Memory using Cadence Virtuoso GPDK 90nm Technology

B.Purna Sai<sup>1</sup>, V.Anand Sree Ram<sup>2</sup>, S.H.V.S.SaiKumar<sup>3</sup>, B.Bhargavi<sup>4</sup>, J. S. Deepika<sup>5</sup>

U.G. Student, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India<sup>1,2,3,4</sup>

Assistant Professor, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India<sup>5</sup>

**ABSTRACT:** Static Random Access Memory (SRAM) is an important semiconductor memory widely used for high-speed applications. It is designed using MOSFET technology because of its low power consumption compared to bipolar transistor technology. Bipolar circuits generate more heat, which limits integration and makes them less suitable for modern designs. The basic SRAM cell initially consists of four transistors, but additional transistors are required for proper read and write operations. This results in the commonly used six-transistor (6T) SRAM cell. The 6T design provides better stability and significantly reduces static power consumption. In contrast, the 4T SRAM cell has continuous current flow, which increases power dissipation. Although the 4T design offers higher density, it introduces fabrication complexity due to the use of resistors. These resistors require additional processing steps and precise design considerations. Advanced SRAM cells such as 8T and 10T are used to improve functionality and performance. These designs support features like multiple ports and better read stability. CMOS technology is preferred in SRAM design to achieve very low power consumption. This is especially important as memory sizes continue to increase in modern systems. Efficient power usage helps in reducing heat generation and improving reliability. Overall, SRAM designed using MOSFETs provides high speed, low power consumption, and scalability, making it ideal for modern electronic applications.

**KEYWORDS:** SRAM , MOSFET, Low Power Consumption ,6T SRAM Cell.

### I. INTRODUCTION

The performance of modern high-performance computing (HPC) systems heavily depends on the efficiency of cache memory. A significant portion of a microprocessor's die area is dedicated to on-chip memory to reduce the latency between the CPU and external storage. This helps in improving overall system speed and performance. Although DRAM provides high density for bulk storage, it is not suitable for cache memory due to its need for periodic refreshing, which slows down operation. As a result, SRAM is widely used in L1 and L2 caches because of its faster speed and simpler control mechanism. With technology scaling down to 90nm, several challenges arise in SRAM design. Increased leakage current leads to higher power consumption even during idle conditions. Additionally, process variations during manufacturing can cause instability in SRAM cells, making them prone to data errors. This project focuses on designing and optimizing SRAM cells to achieve better read stability and write efficiency. The goal is to maintain reliable performance while reducing power consumption, addressing the constraints of modern System-on-Chip (SoC) architectures.

### II. RELATED WORK

Previous research in SRAM design has mainly focused on improving speed, stability, and power efficiency in deep submicron technologies. Traditional memory systems relied on DRAM due to its high density, but its need for periodic refreshing limited its use in high-speed cache applications. This led to the adoption of SRAM as the preferred memory for on-chip caches because of its faster access time and simpler control logic. Early SRAM designs, particularly the 4T cell, provided advantages in terms of area and density. However, they suffered from higher power consumption due to continuous current flow. The presence of resistors also increased fabrication complexity and reduced reliability. To address these limitations, the 6T SRAM cell was introduced, which eliminated static current flow and significantly improved stability and power efficiency. As a result, 6T SRAM became the standard choice in modern VLSI systems. With the scaling of CMOS technology to 90nm, several challenges such as leakage current, short-channel effects, and process variability have emerged, affecting SRAM reliability and performance. These issues become more



## International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

critical in large memory arrays, where even small variations can cause instability. Researchers have focused on improving parameters like Static Noise Margin (SNM) to ensure stable read and write operations. Recent advancements include the use of 8T and 10T SRAM cells to enhance read stability and enable additional features like multi-port access. Moreover, various optimization techniques such as transistor sizing, leakage reduction, and efficient layout design are widely used to improve overall performance. These efforts aim to develop SRAM designs that are low-power, high-speed, and reliable for modern System-on-Chip (SoC) applications.

### III. METHODOLOGY

The proposed methodology for SRAM design follows a structured and hierarchical approach using Cadence Virtuoso in GPDK 90nm technology. Initially, the design begins at the transistor level by properly sizing the 6T SRAM cell to achieve a balance between stability, speed, and power efficiency. At the cell level, the schematic of the SRAM cell is designed and verified for correct functionality in hold, read, and write operations, and after successful validation, it is converted into a symbol to enable hierarchical integration. Pre-layout simulation is then performed using the Spectre simulator to analyze performance parameters such as delay, voltage levels, and power consumption. Following this, the layout design is created using the Virtuoso Layout Editor while strictly following GPDK 90nm design rules to minimize area and parasitic effects. Physical verification steps such as Design Rule Check (DRC) and Layout Versus Schematic (LVS) are carried out to ensure correctness and manufacturability. After verification, parasitic extraction is performed to include real-time resistances and capacitances, and post-layout simulation is conducted to observe performance degradation and ensure reliable operation. Additionally, the methodology includes integration of SRAM cells into rows and complete memory blocks along with decoders and sense amplifiers to form the full SRAM architecture. Simulation strategies such as DC analysis are used to calculate Static Noise Margin (SNM), while transient analysis evaluates read and write delays, and parametric analysis under different temperature conditions is performed to test robustness. This complete design flow ensures that the SRAM cell is stable, efficient, and suitable for modern VLSI applications.

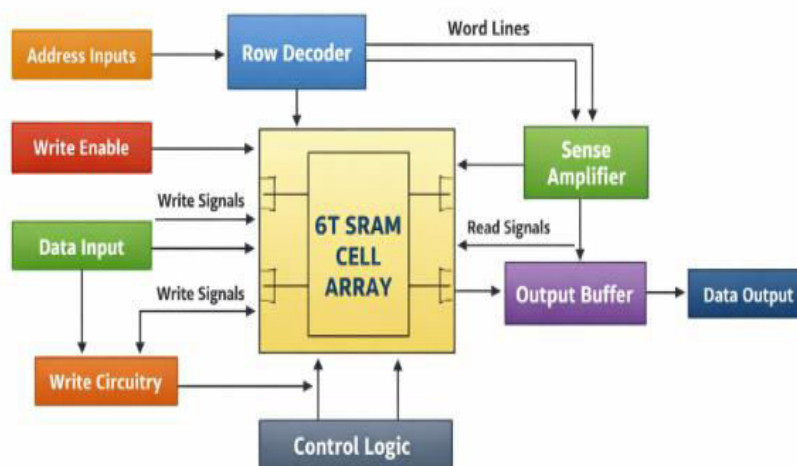


Fig.1 Block Diagram Of 6t Sram Using Cadence Virtuoso Gpdk 90nm Technology

The Fig.1 represents the block diagram of a 6T SRAM memory architecture. It shows how address inputs are decoded by the row decoder to activate specific word lines, allowing access to a particular memory cell in the SRAM array. The write enable signal and data input are processed through the write circuitry to store data into the selected cell. During read operation, the stored data is sensed by the sense amplifier and then passed through the output buffer to produce the final data output. The control logic coordinates all operations, ensuring proper timing and synchronization between read and write processes, making the system efficient and reliable.



## International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

### IV. EXPERIMENTAL RESULTS

The 6T SRAM designed using Cadence Virtuoso in GPDK 90nm technology demonstrate high stability, speed, and power efficiency. The cell achieves a strong Static Noise Margin (SNM) of 420 mV in hold mode and 210 mV in read mode, ensuring reliable data retention. Transient analysis shows fast operation with a read access time of 185 ps and write time of 120 ps, indicating high-speed performance. Power analysis reveals low leakage current of 15 nA per cell and moderate dynamic power of 2.4 mW at 1 GHz. The design successfully passes all functional tests, including read/write operations and disturbance checks, without data corruption. Additionally, it performs reliably across all process corners and temperature variations, confirming robustness and suitability for modern memory applications.

Fig 2:

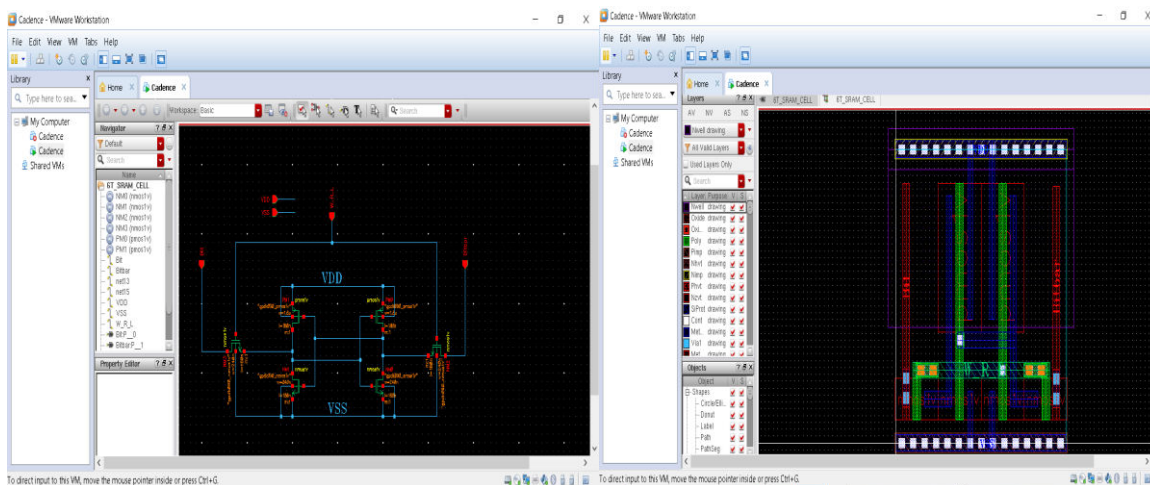


Fig.2.1. Schematic Diagram Of 6t Sram

Fig.2.2. Layout Diagram Of 6t Sram

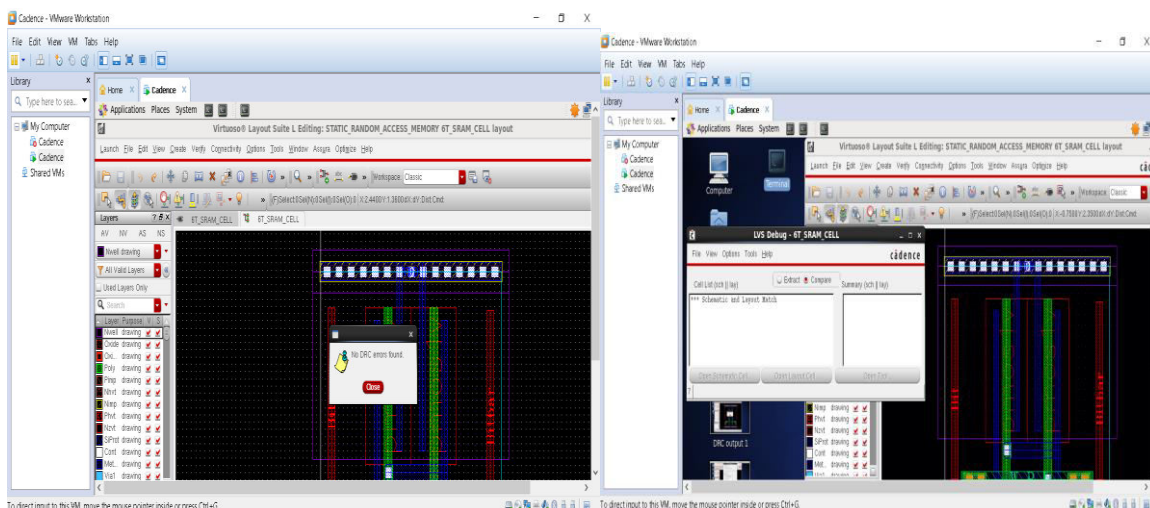


Fig.2.3 Output Of Drc(Design Rule Check)

Fig.2.4 Output Of Lvs(Layout Vs. Schimatic)

Fig.2 shows the results of 6T SRAM Using Cadence Virtuoso GPDK 90nm Technology , Fig.2.1 Schematic Diagram of 6T SRAM, Fig.2.2 Layout Diagram of 6T SRAM, Fig.2.3 Output of DRC, Fig.2.4 Output of LVS



## International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

### V. CONCLUSION

The design and implementation of the 6T SRAM using Cadence Virtuoso in GPDK 90nm technology successfully demonstrates a balance between speed, stability, and power efficiency. The proposed SRAM cell achieves strong data retention with high Static Noise Margin, ensuring reliable operation during read and holds conditions. The design exhibits fast read and write access times, making it suitable for high-speed memory applications. Power analysis confirms low leakage and optimized dynamic power consumption, enhancing overall efficiency. The schematic and layout designs are verified through DRC and LVS, ensuring correctness and fabrication readiness. Functional testing validates accurate read/write operations without data corruption or disturbance. The system performs reliably across various process corners and temperature variations, proving robustness. The hierarchical design approach improves scalability for larger memory arrays. Overall, the project highlights the effectiveness of Cadence tools in VLSI design and verification. Hence, the proposed 6T SRAM design is efficient, reliable, and well-suited for modern integrated circuit applications.

### REFERENCES

- 1) Amit Agarwal, Hai Li and Kaushik Roy." A Single-Vt LowLeakage Gated-Ground Cache for Deep Submicron" IEEE Journal of Solid-state circuits, vol. 38, no. 2, February 2003.
- 2) Singh, S.K., Kaushik, B.K, .and Chauhan, D.S 2013."A novel approach to reduce sub threshold leakage in deep sub-micron SRAM", World Applied Science Journal, vol. 22, no. 3, pp.442-446.
- 3) Anupriya jain "analysis and comparison of leakage reduction techniques for 6T-SRAM and 5T SRAM in 90nm technology" International Journal of engineering Research & technology(IJERT) vol.1 Issue 6,August-2012.
- 4) Kang,S.M and Leblebici,Y.2003.CMOS "Digital Intrigated circuit :Analysis and Design", Third Edition, McGraw-Hill,New York.
- 5) WalidM.Elgharbawy,and,magdy,A.Bayoumi"leakage sources and there possible solution in nm CMOS technologies"IEEE circuit and system magazine fourth quarter 2005.
- 6) Li-Jun Zang,Chen Wu and Ya-Qi Ma,Jian-Binzheng and Ling-Feng Mao "Leakage Power Reduc -tion Technique of 55nm SRAM Cell" IETET Journals, October 07,2011.
- 7) Jun Cheol Park and Vincent J. Mooney III, "Sleepy Stack Leakage Reduction". IEEE Transactions on Very Large Scale Integration (vlsi) Systems", vol. 14, no. 11, November 2006.
- 8) Shaik, S., &Jonnala, P. Performance evaluation of different SRAM topologies using 180, 90 and 45 nm technology. 2013 International Conference on Renewable Energy and Sustainable Energy (ICRESE).
- 9) V.K. Tomar and Ashish Sachdeva"Implementation and Analysis of Power Reduction Techniques in Charge Transfer Sense Amplifier for Sub 90nm SRAM"8thInternational Conference on Computing, Communication and Networking Technologies ICCCNT-2017,held on 3rd -5thJuly- 2017, IEEE -40222, IIT Delhi, NewDelhi.
- 10) Sagar Joshi and SarmanHadia, "Design and Analysis for Low power CMOSSRAM cell in 90nm technology using cadence tool", International Journal of Advanced Research in Computer and Communication Engineering Vol.2,Issue 4, pp.1814- 1817,ApriI2013.



INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA



# INTERNATIONAL JOURNAL OF MULTIDISCIPLINARY RESEARCH IN SCIENCE, ENGINEERING AND TECHNOLOGY

| Mobile No: +91-6381907438 | Whatsapp: +91-6381907438 | [ijmrset@gmail.com](mailto:ijmrset@gmail.com) |

[www.ijmrset.com](http://www.ijmrset.com)